ISO9002 Certified SCI Quality System

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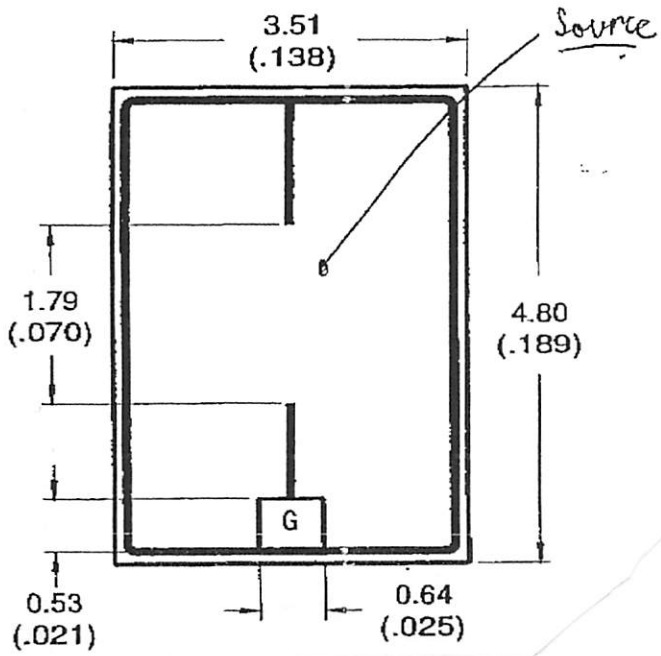
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE	= +/- 0.013
WIDTH	< (.0250) TOLERANCE	= +/- (.0005)
&	> 0.635 TOLERANCE	= +/- 0.025
LENGTH	> (.0250) TOLERANCE	= +/- (.0010)
OVERALL DIE:	< 1.270 TOLERANCE	= +/- 0.102
WIDTH	< (.050) TOLERANCE	= +/- (.004)
&	> 0.635 TOLERANCE	= +/- 0.203
LENGTH	> (.050) TOLERANCE	= +/- (.008)

Topside Metal: Al
Backside: Cr, Ni, Ag
Backside Potential: Drain
Mask Ref: HEX-3.3: 100V, N-Channel, GEN V
Bond Pads : See Above

APPROVED BY: CD **DIE SIZE : .189" x .138"** **DATE: 10/10/03**
MFG: International Rectifier **THICKNESS:** **P/N: IRFC1310N**
"NOTE: This is IR's alternate to the Fairchild RFC40N10